REMARKS

Claims 1, 2 and 4-23 are pending in the application.

Claims 7, 8, 20 and 21 are allowed and claim 2 would be allowed if rewritten in independent form.

Claim 2 is amended to independent form and claim 15 has been cancelled herein.

Independent claim 24 has been newly added. The claim recites a turbo decoder and is fully supported in the specification and figures. No new matter is entered.

Claims 1, 4, 5, 9-11, 14 and 16 have been amended to clarify the claimed invention.

Claims 1, 2, 4, 5, 11 and 23 are objected to for minor informalities. The informalities have been corrected herein.

The drawings are objected to as requiring to designate Figs. 14-17 by a legend "Prior Art." Substitute formal Figs. 14-17 are included herewith.

The previously indicated allowability of claims 1 and 6 is withdrawn in view of the newly cited references to Robertson and Narayanan et al. and Smith et al.

Claim 1 is rejected under 35 U.S.C. 103 as being unpatentable over the published article "Illuminating the Structure of Code and Decoder of Parallel Concatenated Recursive Systematic (Turbo) Codes" by Robertson in view of the published article "A Novel ARQ technique using the Turbo Coding Principle" by Narayanan et al. (Narayanan).

Robertson shows in Fig. 1 the structure of a Turbo-Decoder. However its admitted in the Office Action that Robertson fails to suggest stopping decoding after a fixed number of iterations. However the Office action cites Narayanan for teaching decoding with error detection

and a preset maximum number of iterations before decoding is presumed not possible and an ARQ NACK is sent.

However, applicant's claim 1 includes a unique combination of features not suggested by the combination, nor does the combination teach each and every feature in claim 1.

For example claim 1 includes "first and second elementary decoders for executing....; an error detector for detecting errors in results of the first decoding processing in parallel with a decoding operation of the second decoding processing; and a controller which, when absence of error has been detected in results of the first decoding processing,...."

The combination of references fails to teach all the features in particular the first and second elementary decoders and the controller. Therefore, it is respectfully requested the rejection be withdrawn.

Claims 4, 6, 16-19 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith et al. (6,304,995) (Smith).

Claim 4

Smith teaches an apparatus for iteratively decoding data which has been encoded with concatenated codes. The Office Action refers to Fig. 3 of Smith to show an iterative turbo-decoding system with a single decoding processor. Smith discloses that for an n-iteration decoding scheme the decoder processor 300 must process a decoding iteration n-times as fast as the data is arriving.

However, in contrast to Smith, applicant's claim 4 recites: results of final decoding processing are output from said second elementary decoder directly without intervention of interleaving or deinterleaving.

Smith discloses by reference to Fig. 3, the turbo decoder outputs to the adder which adds the first and second decoding. Therefore the output is the addition of the results of the first and second decoding processing as a decoding result of the turbo decoder.

On the other hand, the turbo decoder of claim 4 outputs the results of the second decoding processing directly without interleaving as a decoding result of the turbo decoder.

Because of the features of applicant's claimed invention, the pattern of generated error contained in a decoded signal is made bursty. As a result, an error rate on a per-information-block basis can be reduced and so can the number of re-sends.

Claims 5, 6, 16-19 and 22

Claim 5 is listed as rejected but is not discussed in the detailed action.

Claims 5 and 6 each include a selection circuit, for example claim 6 recites: a selection circuit for selecting and outputting the results of first and second decoding processing output from said first and second elementary decoders.

The Office Action points to the description of N-iteration decoding, however Smith only makes the statement that the processor must process a decoding iteration n-times as fast when there is n-iteration of decoding. There is no description of a selectable number of iteration decoding and selecting as an output one of the iterations. Nor does Smith describe the selection circuit recited in each of the claims 5 and 6.

In addition the turbo decoder disclosed by Smith outputs to the adder and therefore the output is the addition of the results of the first and second decoding processing as a decoding result of the turbo decoder as pointed out above with respect to claim 4.

Accordingly Smith does not teach a selection circuit of claims 5 and 6 and it is respectfully requested the rejection should be withdrawn.

Similarly <u>claims 17-19 and 22</u>, which include a selector or selecting or as in claim 22 the controlling for selectively outputting, are each different from the cited reference Smith. Smith fails to teach or suggest selecting as described in each of the rejected claims.

<u>Claims 16 and new claim 24</u>:

As pointed out above the decoding result of the turbo decoder disclosed by Smith, outputs from the adder an addition of the results of the first and second decoding processing.

In contrast applicant's claimed the turbo decoder outputs the results of the first <u>or</u> second decoding. Because Smith teaches the output being the addition of the first and second decoding as contrasted to applicants output being the first <u>or</u> second decoding it is submitted the claim is patentably distinguished.

From the foregoing it is respectfully submitted the rejection of claims 5, 6, 16-19 and 22 should be withdrawn. Likewise claim 24 should be allowed.

Because of the unique claimed combination of features in claims 5, 6, 16-19 and 22, the pattern of generated error contained in a decoded signal is made <u>bursty or random as necessary</u>. As a result, error rate on a per-information-block basis can be reduced and so can the number of resends.

<u>Claims 9 and 10</u>

Independent <u>claims 9 and 10</u> are rejected under 35 U.S.C. 102 as being anticipated by Chennakeshu et al. (6,192,503) (Chennakeshu). The Office Action specifically refers to Fig. 5 of Chennakeshu, to show selective recursive decoding of a communications system and col. 9, lines 13-36 of the Chennakeshu disclosure as teaching the limitations of claims 9 and 10.

However applicant's claims 9 and 10 include an error detector detects errors <u>in parallel</u> with a current decoding operation. Specifically, for example, claim 9 includes: detecting errors

in results of previous decoding in parallel with a current decoding operation in the iterative decoding processing; and a controller which, when absence of error has been detected in the results of the previous decoding, is operable for outputting the results of the previous decoding and halting the current decoding operation.

By reference to Chennakeshu's Fig. 9, first decoding processing is executed at step 920, subsequently whether predetermined reliability criterion is satisfied or not is judged at step 930, then second decoding processing is executed at step 940 based upon the results of the judgment.

However according Chennakeshu's Fig. 9, this judgment is not executed in parallel with the second decoding processing. Therefore it is respectfully submitted Chennakeshu does not teach an error detector of claims 9 and 10 detects errors in parallel with a current decoding operation.

For at least the foregoing reasons it is respectfully requested the rejection of claims 9 and 10 be withdrawn.

Claims 11, 14 and 23 are rejected under 35 U.S.C. 102 (e) as being anticipated by Zhang et al. (6,233,709) (Zhang). The Office Action refers to Fig. 3 of Zhang as disclosing all the features of claims 11, 14 and 23. Zhang teaches an iterative decoder in which the number of iterations N are dynamically adjusted within a certain range.

The Office Action asserts decision circuitry 118 as shown in Fig. 1 of Zhang describes the performing a CRC check of applicant's claim 11. However, Zhang teaches that the CRC check is executed using results of the second decoding processing.

Unlike Zhang, the error detector of applicant's claim 11 detects errors in the results of the first decoding processing. Thus Zhang is different from applicant's claimed invention of claim 11.

Claims 14 includes: a decoder for executing the first and second decoding processing and executing the second decoding processing using a signal obtained by interleaving the results of the first decoding processing; controlling the decoder so that the first decoding processing is executed and then the second decoding processing is executed.

Unlike the claimed invention, the turbo decoder disclosed by Zhang uses first and second constituent decoders 104 and 112. Thus Zhang fails to teach a single decoder and controlling the decoder as claimed in 14 since neither decoder in Zhang executes the first and second decoding processing.

The turbo decoder of claim 14 uses a single decoder for executing the first and second decoding processing and the controller in controlling the single decoder is not found in the Zhang reference.

It is respectfully submitted Zhang fails to teach using the single decoder and the controller as disclosed in claim 14.

Claim 23 recites a controller which is different from the features described in the Zhang reference. The controller controls decoding processing so that the second decoding processing is executed using a signal obtained by deinterleaving the results of the first decoding processing in a case where the turbo decoder executes decoding for each unit of the turbo code including a plurality of information blocks.

In a case where the turbo code includes a plurality of information blocks, according to claim 23, the pattern of generated error contained in a decoded signal is not made random, but made bursty. As a result, an error rate on a per-information-block basis can be reduced.

It is respectfully submitted Zhang fails to teach using the single decoder and the controller as disclosed in claim 23.

Claims 15, 17, 18, 22 and 23 are rejected under 35 U.S.C. 102 (a) as being anticipated by the published article by Hong et al. (Hong).

Claim 15 has been cancelled herein.

Applicant's claims 17 and 22 recite the selector and controller. As previously pointed out above the claims include selecting and outputting one of the results of the first and second decoding processing.

Hong appears to disclose a decoder. But the decoder does not have a function that selectively outputs the results of the first or second decoding processing.

It is respectfully submitted that Hong does not disclose the selector and controller of the respective claims 17 and 22. That is, the decoder disclosed by Hong does not have the functions as recited in each of claims 17 and 22.

Claim 23 recites a controller which is different from the features described in the Hong reference. The controller controls decoding processing so that the second decoding processing is executed using a signal obtained by deinterleaving the results of the first decoding processing in a case where the turbo decoder executes decoding for each unit of the turbo code including a plurality of information blocks.

In a case where the turbo code includes a plurality of information blocks, according to claim 23, the pattern of generated error contained in a decoded signal is not made random, but made bursty. As a result, an error rate on a per-information-block basis can be reduced.

Claims 11-13 are rejected under 35 U.S.C. 102 (e) as being anticipated by Pyndiah et al. (6,122,763) (Pyndiah). The Office Action again refers to Fig. 6 of Pyndiah et al. as showing subject matter of claims 11-13.

Applicant's claim 11 recites a turbo decoder which includes outputting the results of the first decoding processing stored in said memory in accordance with the result of the error detection.

In contrast Pyndiah, as shown in Fig. 3, does not have a function that outputs results of the first decoding processing. It is respectfully submitted that Pyndiah does not teach the claimed invention and claims 11-13 are allowable.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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